Karnatak Law Society’s

GOGTE INSTITUTE OF TECHNOLOGY

Udyambag Belagavi -590008

Karnataka, India.



A Course Project Report on

**“4-Bit Even Parity Checker”**

Submitted for the requirements of 3rd semester B.E. in CSE

for **“Digital Electronics** (18CS33)**”**

**Submitted by**

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**Under the guidance of**

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Karnatak Law Society’s

GOGTE INSTITUTE OF TECHNOLOGY

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Karnataka, India.

Department of CSE

Academic Year 2021-2022 (Odd semester)



**Certificate**

This is to certify that the Course Project work titled **“4-Bit Even Parity Checker”** for **“Digital Electronics** (18CS33)**”**carried out by Students: SHRADHA MALLIKARJUN PATIL (2GI20CS144), SRUSHTI B MUDENNAVAR (2GI20CS158), SUSHMITA G KULALI (2GI20CS163), VANI F DODAMANI (2GI20CS172) have submitted in partial fulfilment of the requirements for 3rd semester B.E. in COMPUTER SCIENCE AND ENGINEERING, Visvesvaraya Technological University, Belagavi. It is certified that all corrections/suggestions indicated have been incorporated in the report. The course project report has been approved as it satisfies the academic requirements prescribed for the said degree.

Date:31-01-2022 Signature of Guide

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MARKS ALLOCATION:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **Batch No.:** | | | | | |
| 1. | Seminar Title: | Marks Range | **USN** | | | |
| **2GI20CS144** | **2G20CS158** | **2GI20CS163** | **2GI20CS172** |
| 2. | Abstract (PO2) | 0-2 |  |  |  |  |
| 3. | Application of the topic to the course (PO2) | 0-3 |  |  |  |  |
| 4. | Literature survey and its findings (PO2) | 0-4 |  |  |  |  |
| 5. | Methodology, Results and Conclusion  (PO1, PO3, PO4) | 0-6 |  |  |  |  |
| 6. | Report and Oral presentation skill (PO9, PO10) | 0-5 |  |  |  |  |
|  | Total | 20 |  |  |  |  |

**\* 20 marks is converted to 10 marks for CGPA calculation**

**1.Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.

**2.Problem Analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and Engineering sciences.

**3.Design/Development of solutions:**Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

**4.Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

**5.Modern tool usage:**Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

**6.The engineer and society:**Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

**7.Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need

for sustainable development.

**8.Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

**9.Individual and team work:** Function effectively as an individual and as a member or leader in diverse teams, and in multidisciplinary settings.

**10.Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

**11. Project management and finance:** Demonstrate knowledge and understanding of the engineering management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

**12. Life-long learning:** Recognize the need for and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

**Signature of Staff**

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INTRODUCTION:

In [digital electronic](https://technobyte.org/digital-electronics-logic-design-course-engineering/) systems, during data transmission and processing, data gets distorted. This is due to the noises added to it. Such noises change 0s to 1s and 1s to 0s.

The parity generating technique is one of the most widely used error detection techniques for the data transmission. In digital systems, when binary data is transmitted and processed, data may be subjected to noise so that such noise can alter 0s (of data bits) to 1s and 1s to 0s.

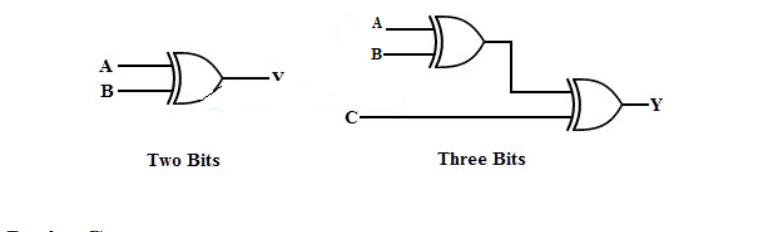
Hence, a Parity Bit is added to the word containing data in order to make number of 1s either even or odd. The message containing the data bits along with parity bit is transmitted from transmitter to the receiver.

At the receiving end, the number of 1s in the message is counted and if it doesn’t match with the transmitted one, it means there is an error in the data. Thus, the Parity Bit it is used to detect errors, during the transmission of binary data.

PARITY CHECKER:

It is a logic circuit that checks for possible errors in the transmission. This circuit can be an even parity checker or odd parity checker depending on the type of parity generated at the transmission end. A parity generator is a combinational logic circuit that generates the parity bit in the transmitter. On the other hand, a circuit that checks the parity in the receiver is called parity checker. A combined circuit or devices of parity generators and parity checkers are commonly used in digital systems to detect the single bit errors in the transmitted data word. The sum of the data bits and parity bits can be even or odd. In even parity, the added parity bit will make the total number of 1s an even amount whereas in odd parity the added parity bit will make the total number of 1s odd amount.

The basic principle involved in the implementation of parity circuits is that sum of odd number of 1s is always 1 and sum of even number of 1s is always zero. Such error detecting and correction can be implemented by using Ex-OR gates (since Ex-OR gate produce zero output when there are even number of inputs). To produce two bits sum, one Ex-OR gate is sufficient whereas for adding three bits two Ex-OR gates are required as shown in below figure.

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WORKING OF A PARITY GENERATOR:

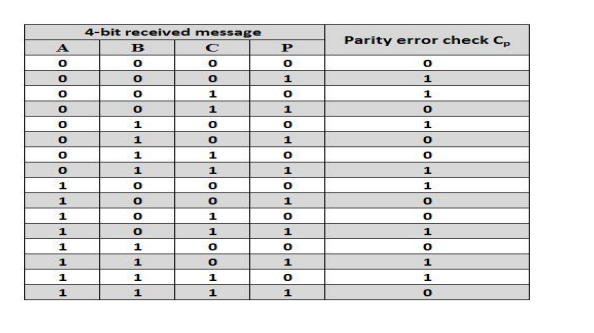
Assume that your final message is an n-bit stream of digital data. One of the bits is the parity bit. To transmit this bitstream containing n-1 data (message signal) plus one additional parity bit, we require a special circuit known as parity bit generator. The parity generator is a [combinational logic circuit](https://technobyte.org/sequential-combinational-logic-circuits-types/).

The parity generators can create two parities. Even parity generates a final message with an even number of 1s. So the parity bit for an even number of 1s is 0. On the other hand, an odd parity bit generates when the total number of 1s in the bitstream is odd.

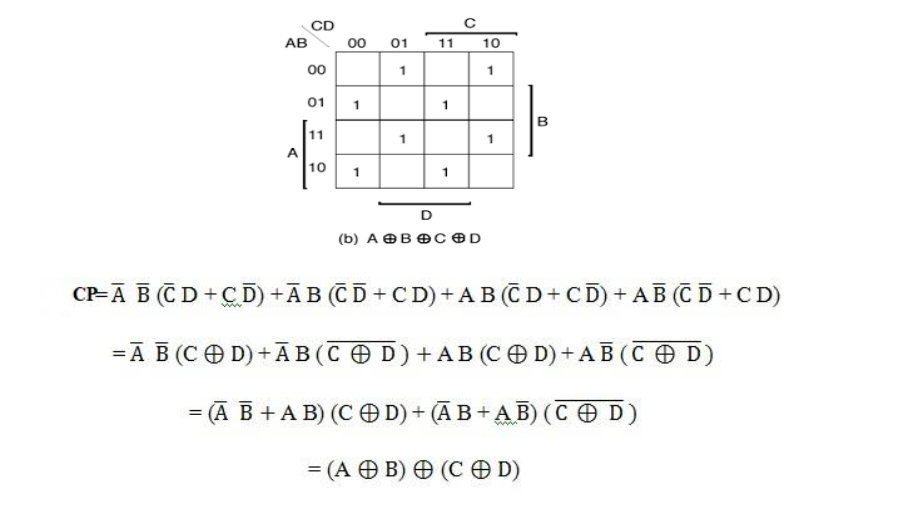
4-BIT EVEN PARITY GENERATOR:

Even Parity Checker Consider that three input messages along with even parity bit is generated at the transmitting end. These 4 bits are applied as input to the parity checker circuit which checks the possibility of error on the data. Since the data is transmitted with even parity, four bits received at circuit must have an even number of 1s. If any error occurs, the received message consists of odd number of 1s. The output of the parity checker is denoted by PEC (parity error check). The below table shows the truth table for the even parity checker in which PEC = 1 if the error occurs, i.e., the four bits received have odd number of 1s and PEC = 0 if no error occurs, i.e., if the 4-bit message has even number of 1s.

TRUTH TABLE:

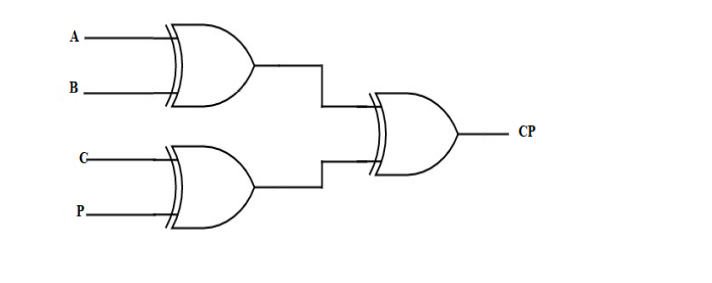
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K-MAP:

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LOGIC DIAGRAM:

The above logic expression for the even parity checker can be implemented by using three Ex-OR gates as shown in figure. If the received message consists of five bits, then one more Ex-OR gate is required for the even parity checking.



CONCLUSION:

The parity generator generates the parity bit in the transmitter and the parity checker checks the parity bit in the receiver.

The parity checker is needed to detect the errors in communication and also in the memory storage devices parity checker is used for testing.

The parity bit is also used in Small Computer System Interface (SCSI) and also in Peripheral Component Interconnect (PCI) to detect the errors

REFERENCES:

1. Donald P Leach, Albert Paul Malvino and GoutamSaha: Digital Principles and Applications, 7th Edition and onwards, Tata McGraw Hill, 2011.
2. <https://technobyte.org/parity-generator-parity-checker/>